ABSTRACT

A honeycomb/webbed, high surface area capacitor formed by etching a storage poly using an etch mask having a plurality of micro vias. The etch mask is preferably formed by applying an HSG polysilicon layer on a surface of the storage poly with a mask layer being deposited over the HSG polysilicon layer. An upper portion of the mask layer is removed to expose the ~~upper-most~~ upper-most portions of the HSG polysilicon layer and the exposed HSG polysilicon layer portions are then etched, which translates the pattern of the exposed HSG polysilicon layer portions into the storage poly. The capacitor is completed by depositing a dielectric material layer over the storage poly layer and depositing a cell poly layer over the dielectric material layer.